REMARKS

The claims are claims 1 to 7.

The application has been further amended at many locations to correct minor errors and to present uniform language throughout. The amendments include a further update of the status of two of the copending applications cited on page 1. The amendments include correction of a spelling mistake at page 5, line 8. The amendments include correction of the reference numbers cited at page 11, lines 3 to 15 to correspond to corrected Figure 4. The amendments include correction of "digital frame counter" to "debug frame counter" at page 14, line 15, page 15, lines 1, 7, 21, 24 and 27, and page 16, lines 2, 3, 15 and 17. This corrects an error in the original application. This amendment also includes further change to page 18, lines 13 and 14.

The amendment filed September 18, 2004 was objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. The FINAL REJECTION notes the following alleged new matter: the amended sentence at page 18, lines 13 and 14; amended steps of "incrementing" and "decrementing" in claim 1; and added new claims 4 and 5.

Page 18, lines 13 to 14 has been further amended. The sentence originally reading "The address comparison unit 310 generates a debug suspend request when the ACNTL register ASTOP and AFEN bits are TRUE." has been amended to read "The address comparison unit 310 generates a debug suspend request." This amended language is not contrary to the original disclosure as the Examiner stated at paragraph 6-1 of the FINAL REJECTION. Rather the amended language is general where the original language was specific. However, the amended language and the original language are completely consistent with each other. The original application referenced ASTOP and AFEN bits only in this section.

Because the Examiner ruled this subject matter was not sufficiently described under 35 U.S.C. 112, first paragraph, these references are deleted. The original rejection in effect stated that reference to AFEN was meaningless. By rejecting the deletion as new matter, the Examiner is saying that deletion of a meaningless phrase introduces new matter. The Applicant respectfully submits that the amended language does not introduce new matter.

The amended recitations in the "incrementing" and "decrementing" steps of claim 1 is not new matter. The original application employed two terms "debug frame counter" and "digital frame counter" for the same structure. All references to "digital frame counter" have been changed to "debug frame counter." Study of all references to these terms indicates their identity. The disclosure of incrementing the digital frame counter on each high priority at page 14, line 15 corresponds to disclosure of incrementing the debug frame counter at page 5, lines 7 to 8, page 17, lines 2 to 3 and page 29, lines 18 to 21. The disclosure of decrementing the digital frame counter on return from interrupt at page 15, lines 1 and 21 corresponds to disclosure of decrementing the debug frame counter at page 5, lines 7 to 8, page 17, lines 3 to 4 and page 29, lines 18 to 21. The disclosure regarding the meaning of a digital frame counter equal to zero at page 15, line 7, page 16, lines 2 and 17 correspond to disclosure regarding the debug frame counter at page 16, line 32 to page 17, line 2 and page 29, lines 12 to 13. The disclosure that the digital frame counter indicates the interrupt level at page 15, line 24 corresponds to similar teaching about the debug frame counter at page 5, lines 16 to 18. The disclosure about reading the digital frame counter at page 15, line 27 corresponds to teaching about the debug frame counter at page 29, lines 21 to 24. Figure 6 illustrates a debug frame counter while the application does not state any figure illustrates a digital frame counter.

With these corrections, the limitation in claim 1 "incrementing a debug frame counter upon each of the at least one type interrupt received while suspending normal program execution" is disclosed in the application at: page 5, lines 5 to 8 (real time interrupt); page 14, lines 15 and 16 (high priority interrupt); page 17, lines 2 and 3; and page 29, lines 18 to 21. The limitation in claim 1 "decrementing the debug frame counter upon each return from interrupt received while suspending normal program execution" is disclosed in the application at: page 5, lines 5 to 8 (real time interrupt); page 15, lines 1 and 2; page 15, lines 20 and 21; page 17, lines 3 and 4; and page 29, lines 18 to 21. This subject matter is also taught in the ABSTRACT at page 32, lines 5 to 7. Accordingly, the amended language of claim 1 is not new matter.

Claim 4 has been amended to conform to the original disclosure. As amended, claim 4 recites the integrated circuit includes "a plurality of emulation peripherals, each emulation peripheral including a plurality of debug event detectors" and the method further comprises "limiting each of said emulation peripherals to triggering a single debug event before being cleared." The application states at page 29, lines 7 to 9 that each emulation peripheral includes plural debug event detectors and cites address comparison unit 310, data comparison unit 320 and external comparison unit 330, which are illustrated in Figure 7. Limiting an emulation peripheral to a single debug event before being cleared is disclosed at page 29, lines 25 to 32.

Claims 1 to 7 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. The FINAL REJECTION cites: amendment to the specification deleting

AFEN as setting an new condition for operation of address comparison unit 310 not disclosed in the original application: the amended "incrementing" and "decrementing" steps of claim 1 regarding "at least one type interrupt" and "received during normal program execution" as not disclosed in the original application; and new claims 4 and 5 as not disclosed in the original application.

The Applicant respectfully submits that the amendment deleting AFEN does not make the application inadequate to teach the claimed invention. The operative limitations in claim 1 are "detecting a first debug event" and "detecting at least one second debug event." The application discloses at page 17, line 5 to page 29, line 6 and illustrates in Figure 7 circuits including address comparison unit 310, data comparison unit 320 and external comparison unit 330. The operation of address comparison unit 310 is described at page 17, line 19 to page 22, line 22. This disclosure makes clear that address comparison unit 310 receives a bus input from multiplexer 311 (page 18, lines 6 to 8) and generates events signals (page 18, lines 9 to 12). This disclosure teaches that address comparison unit 310 operates in three modes: event generation (page 18, line 9 to page 19, line 15); counter functions (page 19, line 16 to the end of Table 3 on page 21) and parallel signature analysis (page 22, lines 1 to 22). The disclosure makes clear that the output type is the same for these three modes. The complained text of page 18 only concerns the event generation mode, just one of three modes described. The current amendment merely changes a specific limitation that is not completely described to a general limitation including the specific limitation. Thus the amended description of address comparison unit 310 is proper under 35 U.S.C. 112.

The application is sufficient under 35 U.S.C. 112 even in the absence of any description of address unit 310. As noted above, this application also describes data comparison unit 320 and

external comparison unit 330. These structures are adequate to support the limitations of claim 1. Accordingly, the amended description is proper under 35 U.S.C. 112.

The description of the "incrementing" and "decrementing" in claim 1 is proper under 35 U.S.C. 112. As noted above, the term "digital frame counter" has been amended to "debug frame counter" throughout the application. With these corrections, the limitation in claim 1 "incrementing a debug frame counter upon each of the at least one type interrupt received while suspending normal program execution" is disclosed in the application at: page 5, lines 5 to 8 (real time interrupt); page 14, lines 15 and 16 (high priority interrupt); page 17, lines 2 and 3; and page 29, lines 18 to 21. The limitation in claim 1 "decrementing the debug frame counter upon each return from interrupt received while suspending normal program execution" is disclosed in the application at: page 5, lines 5 to 8 (real time interrupt); page 15, lines 1 and 2; page 15, lines 20 and 21; page 17, lines 3 and 4; and page 29, lines 18 to 21. This subject matter is also taught in the ABSTRACT at page 32, lines 5 to 7. Accordingly, the amended language of claim 1 is proper under 35 U.S.C. 112.

Claims 4 and 5 are proper under 35 U.S.C. 112. Claim 4 has been amended to conform to the original disclosure. As amended, claim 4 recites the integrated circuit includes "a plurality of emulation peripherals, each emulation peripheral including a plurality of debug event detectors" and the method further comprises "limiting each of said emulation peripherals to triggering a single debug event before being cleared." The application states at page 29, lines 7 to 9 that each emulation peripheral includes plural debug event detectors and cites address comparison unit 310, data comparison unit 320 and external comparison unit 330, which are illustrated in Figure 7. Limiting an emulation peripheral to a single debug event before being

cleared is disclosed at page 29, lines 25 to 32. Thus claims 4 and 5 are proper under 35 U.S.C. 112.

Claims 1 to 7 were rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The alleged inadequate description of the AFEN bit does not make the application inadequate to describe the limitations of claims 1 to 7. This application teaches event generation by address comparison unit 310, data comparison unit 320 and external comparison unit 330. The alleged inadequacy of description of address unit 310 does not negate the description of data comparison unit 320 and external comparison unit 330. The description of data comparison unit 320 and external comparison unit 330 are adequate to support the limitations of claims 1 to 7. Further, the alleged inadequacy of the description of address comparison unit 310 does not negate the disclosure of two other modes of operation of address comparison unit 310. Finally, even the allegedly flawed description of address comparison unit 310 makes clear that it compares a bus input selected by multiplexer 311 with data in a AREF register as masked by an address mask in the AMSK register. This disclosure alone is sufficient to support the claimed limitations. Note that the claims do not require any detail regarding the AFEN bit, thus lack of adequate description of this bit does not make the disclosure inadequate.

Some pages referenced in the previous response were incorrect. The correct references are as follows. The limitation of "incrementing a debug frame counter upon each of the at least one type interrupt received while suspending normal program execution" is described in the application at: page 5, lines 5 to 8; page 14, lines 15 to 16; page 17, lines 2 and 3; and page 29, lines 18 to

21. The limitations of claim 2 are described in the application at: page 5, lines 4 to 7; page 5, lines 9 to 11; page 5, lines 13 to 17; page 12, lines 17 to 23; page 13, line 27 to page 14, line 6; page 29, lines 10 to 13; page 29, lines 21 to 24; page 29, lines 26 to 29; page 32, lines 11 to 14. Note the application distinguishes between debug events that cause transition from execute state 101 to debug suspend state 102 (Figure 5, page 12, lines 17 to 18) and high priority interrupts that cause transition from debug suspend state 102 to interrupt during suspend state 103 (Figure 5, page 13, line 17 to page 14, line 4). The limitations of claim 3 are described in the application at: page 5, lines 16 to 18; page 15, line 27 to page 16, line 7; and page 29, line 21 to 24.

The FINAL REJECTION complains the most claim limitations exist in only the ABSTRACT and SUMMARY OF THE INVENTION. The Applicant disputes that this is true. This response cites many other parts of the application teaching the claimed limitations. Further, even if true this does not make the teaching of the application inadequate. There is no allegation that a limitation taught only in the ABSTRACT and SUMMARY OF THE INVENTION is insufficiently taught in the application or that the teachings of the ABSTRACT and SUMMARY OF THE INVENTION are improper under 35 U.S.C. 112. The Applicant requests the Examiner cite a particular limitation allegedly not adequately described or withdraw this objection.

The plurality of debug event detectors recited in claim 2 is described in the application at page 17, line 5 to page 29, line 6 and illustrated in Figure 7. The application states that the circuits of Figure 7 are "located on each megamodule concerned with emulation." Since Figure 3 illustrates plural such megamodules, there are plural debug event detectors.

The recitations of claim 1 are proper in light of the teachings of the application. The application states at page 12, lines 23 to

25 "In general, debug events are allowed at an instruction boundary, when reset is inactive and no interrupts are active." This "In general" would be understood as meaning usual or customary. Note that the application states certain interrupts are permitted during debug suspend state 102. The application states at page 13, line 27 to page 13, line 6:

> "Certain interrupts transit the operation state from debug suspend state 102 to interrupt during suspend (IDS) state 103. These interrupts are defined by a separate interrupt mask independent of the normal interrupt mask. Those interrupts defined as high priority interrupts (HPI) or foreground interrupts cause the operation state to enter the interrupt during suspend state 103 from the debug suspend state 102. The debug suspend state 102 enables high priority interrupts independent of the state of the global interrupt enable bit or of software run directives. This enables debugging of background tasks while the target device 3 continues to service a real time application via high priority interrupts."

This specific description of a particular type interrupt permitted during the debug suspend state 102 overrules the "In general" recitation cited by the Examiner. Accordingly, the recitations of claim 1 are proper.

The Applicants respectfully request entry and consideration of this amendment. Entry of this amendment is proper at this time because the amendment serves only to clarify subject matter previously recited. Thus no new search or reconsideration is required.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early entry of this amendment, reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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